ASAP 2021 Poster Session II

Poster 2.1. **“A Low Power Branch Prediction for Deep Leaning on RISC-V Processor”**

Mingjian Sun, Yuan Li, Song Chen and Yi Kang, *University of Science and Technology of China, China*

Poster 2.2. **“Parallel Construction of Independent Spanning Trees on Folded Crossed Cubes”**
Huanwen Zhang, Yan Wang, Jianxi Fan and Ruyan Guo, *Soochow University, China*

Poster 2.3. “**IMAX2: A CGRA with FPU + Multithreading + Chiplet**”

Tomoya Akabe and Hidenari Inamasu, *Nara Institute of Science and Technology, Japan*

Poster 2.4. “**Compilation and Optimization Techniques for Coarse-Grained Reconfigurable Architectures**”
Takuya Kojima, *Keio University, Japan*

Paper 4.1 "**Number Theoretic Transform Architecture suitable to Lattice-based Fully-Homomorphic Encryption**"
Rogério Paludo and Leonel Sousa, *INESC-ID, Instituto Superior Técnico, Universidade de Lisboa, Portugal. Portugal*

Paper 4.2 "**ABACa: Access Based Allocation on Set Wise Multi-Retention in STT-RAM Last Level Cache**"
Sukarn Agarwal and Shounak Chakraborty, *Indian Institute Of Technology (BHU) Varanasi, India*

Paper 4.3 "**DARM: A Low-Complexity and Fast Modular Multiplier for Lattice-Based Cryptography**"
Xiao Hu, Minghao Li, Jing Tian and Zhongfeng Wang, *Nanjing University, China*

Paper 4.4 "**XDIVINSA: eXtended DIVersifying INStruction Agent to Mitigate Power Side-Channel Leakage**"
Thinh Hung Pham, Ben Marshall, Alexander Fell, Siew-Kei Lam and Daniel Page, *University of Bristol, Department of Computer Science, UK*

Paper 4.5 "**Memory-aware Efficient Deep Learning Mechanism for IoT Devices**"
Jishnu Banerjee, Sahidul Islam, Wei Wei, Chen Pan, Dakai Zhu and Mimi Xie, *University of Texas at San Antonio, USA*

Paper 4.6 "**AERO: Towards Energy-Efficient Autonomous Flight in MAVs Using Approximate Execution**"
Ben Li, Jingweijia Tan and Kaige Yan, *Jilin University, China*

Paper 6.1 "**ASBNN: Acceleration of Bayesian Convolutional Neural Networks by Algorithm-hardware Co-design**"
Yoshiki Fujiwara and Shinya Takamaeda-Yamazaki, *The University of Tokyo, Japan*

Paper 6.2 "**A novel Ring-based small-world NoC for Neuromorphic Processor**"
Yuchen Qiu, Chao Xiao, Linghui Peng, Junhui Wang, Ziyang Kang, Shiming Li and Lei Wang, *National University of Defense Technology, China*

Paper 6.3 "**Double-Pumping the Interconnect for Area Reduction in Coarse-Grained Reconfigurable Arrays**"
Xinyuan Wang, Tianyi Yu, Hsuan Hsiao and Jason Anderson, *University of Toronto, Canada*

Paper 6.4 "**An Efficient Hardware Architecture for Sparse Convolution using Linear Feedback Shift Registers**"
Murad Qasaimeh, Joseph Zambreno and Phillip Jones, *Iowa State University, USA*

Paper 6.5 "**WinoCNN: Kernel Sharing Winograd Systolic Array for Efficient Convolutional Neural Network Acceleration on FPGAs**"
Xinheng Liu, Yao Chen, Cong Hao, Ashutosh Dhar and Deming Chen, *University of Illinois at Urbana-Champaign, USA*

Paper 6.6 "**FlexACC: A Programmable Accelerator with Application-Specific ISA for Flexible Deep Neural Network Inference**"
En-Yu Yang, Tianyu Jia, David Brooks and Gu-Yeon Wei, *Harvard University, USA*