Prof. Subhasish Mitra
Dept. of Electrical Engineering and Dept. of Computer Science
Stanford University

Title: **21st-Century NanoSystems for Abundant-Data Computing: The *N3XT 1,000X***

Abstract:
The world's needs for analyzing massive amounts of data is growing dramatically. The computation demands of these abundant-data applications, such as AI machine learning, far exceed the capabilities of today's computing systems. For example, a Dream AI Chip would co-locate all memory on a single chip together with computing elements, quickly accessible at low energy. Such Dream Chips aren't realizable today. Computing systems instead use large off-chip memory and spend enormous time and energy shuttling data back-and-forth. This memory wall gets worse with growing problem sizes, especially as conventional transistor miniaturization gets increasingly difficult.

This talk will present the *N3XT* (Nano-Engineered Computing Systems Technology) approach to build transformative NanoSystems by exploiting unique properties of underlying nanotechnologies. *N3XT* creates new chip architectures for computation immersed in memory through ultra-dense (monolithic) 3D integration of new logic devices (such as
carbon nanotube transistors for high-speed and low-energy circuits) and new non-volatile memory (such as dense resistive RAM that can store multiple bits inside each memory cell). To scale with growing problem sizes, new Illusion systems orchestrate multiple *N3XT* chips to create an illusion of a Dream Chip with near-Dream energy and throughput.

A wide variety of *N3XT* hardware prototypes, built in commercial and research facilities, represent leading examples of transforming scientifically interesting nanomaterials and nanodevices into actual 21st-century NanoSystems. *N3XT* NanoSystems target 1,000X system-level energy-delay-product benefits especially for abundant-data applications. Such massive benefits enable coming generations of applications that push new frontiers, from deeply-embedded computing systems all the way to the cloud.

Bio:

Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He directs the Stanford Robust Systems Group, leads the Computation Focus Area of the Stanford SystemX Alliance, and is a member of the Wu Tsai Neurosciences Institute. Prof. Mitra also holds the Carnot Chair of Excellence in NanoSystems at CEA-LETI in France. His research ranges across Robust Computing, NanoSystems, Electronic Design Automation (EDA), and Neurosciences. Results from his research group have influenced almost every contemporary electronic system, and have inspired significant government and research initiatives in multiple countries. Prof. Mitra also has consulted for major technology companies including Cisco, Google, Intel, Samsung, and Xilinx.

In the field of Robust Computing, he has created many key approaches for circuit failure prediction, on-line diagnostics, QED system validation, soft error resilience, and X-Compact test compression. Their adoption by industry is growing rapidly, in markets ranging from cloud computing to automotive systems. His X-Compact approach has proven essential for cost-effective manufacturing and high-quality testing of almost all 21st century systems, enabling billions of dollars in cost savings.

With his students and collaborators, he demonstrated the first carbon nanotube computer. They also demonstrated the first 3D NanoSystem with computation immersed in data storage. These received wide recognition: cover of NATURE, Research Highlight to the US Congress by the NSF, and highlight as "important, scientific breakthrough" by global news organizations.

Prof. Mitra's honors include the Newton Technical Impact Award in EDA (test of time honor by ACM SIGDA and IEEE CEDA), the Semiconductor Research Corporation's Technical Excellence Award, the Intel Achievement Award (Intel's highest honor), and the US Presidential Early Career Award. He has published award-winning papers at major venues such as the Design Automation Conference, International Solid-State Circuits Conference, International Test Conference, Symposium on VLSI Technology, and Formal Methods in Computer-Aided Design. Stanford undergraduates have honored him several times "for being important to them." He is an ACM Fellow and an IEEE Fellow.